AMENDMENTS TO THE CLAIMS

Claims 1-8. (Canceled)

9. (Previously presented) A method of forming a memory device, comprising the steps of:

forming at least one in-pixel gate structure in an array region of a substrate, said at least one in-pixel gate structure being further formed by providing a first doped conductive layer over said substrate and providing a first silicide region over said first doped conductive layer;

forming at least one peripheral gate structure in a peripheral region of said substrate, said peripheral region being adjacent said array region, said at least one peripheral gate structure being further formed by providing a second doped conductive layer over said substrate and providing a second silicide region over said second doped conductive layer; and

forming at least one capacitor structure over an isolation region in said array region, said at least one capacitor structure being further formed by providing a first capacitor electrode layer, providing a dielectric layer over said first capacitor electrode layer, and providing a second capacitor electrode layer over said dielectric layer, wherein said steps of providing said first and second silicide regions are conducted subsequent to said step of providing said second capacitor electrode layer.

10. (Original) The method of claim 9, wherein said first and second doped conductive layers are formed of polysilicon.

11. (Original) The method of claim 9, wherein said second capacitor electrode layer is formed of doped polysilicon.

12. (Original) The method of claim 11, wherein said undoped polysilicon is formed by deposition at a temperature between about 600ºC to about 800ºC.

13. (Currently amended) A method of forming a memory cell, comprising the steps of:

forming a transistor including a gate fabricated on a semiconductor substrate ~~and including a source/drain region in said semiconductor substrate disposed adjacent to said gate~~, said step of forming said transistor including providing a silicide region of said gate; [[and]]

forming a capacitor adjacent said transistor by providing a first conductive layer, a dielectric layer and a second conductive layer, wherein said steps of providing said first conductive layer, said dielectric layer and said second conductive layer are conducted prior to said step of providing said silicide region of said gate; and

forming source/drain regions in said semiconductor substrate disposed adjacent to said gate, said step of forming said source/drain regions being conducted subsequent to said step of forming said silicide region of said gate.

14. (Original) The method of claim 13, wherein said first conductive layer is formed of doped polysilicon.

15. (Previously presented) The method of claim 13, wherein said second conductive layer is formed of doped polysilicon.

16. (Original) The method of claim 15, wherein said second conductive layer is formed by deposition at a temperature between about 600ºC to about 800ºC.

17. (Original) The method of claim 13, wherein said step of providing said silicide region of said gate includes providing a metal layer a gate electrode and annealing said metal layer to form said silicide layer.

18. (Original) The method of claim 13, wherein said transistor is a MOSFET.

19. (Original) The method of claim 13, wherein said semiconductor substrate is a silicon substrate.

20. (Original) The method of claim 13, wherein said memory cell is a DRAM.

21. (Original) The method of claim 13, wherein said memory cell is one of a DRAM, flash memory or SRAM.

Claims 22-45. (Canceled)

46. (Previously presented) The method of claim 9, wherein the memory device is a DRAM device.